- 2-V to 6-V V_{CC} Operation
- Inputs Accept Voltages to 6 V
- Max t_{pd} of 9.5 ns at 5 V
- 3-State Noninverting Outputs Drive Bus Lines Directly
- Full Parallel Access for Loading

SN54AC373 . . . J OR W PACKAGE
SN74AC373 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)

```
        ___
 OE  [ 1    20 ] V_CC
 1Q  [ 2    19 ] 8Q
 1D  [ 3    18 ] 8D
 2D  [ 4    17 ] 7D
 2Q  [ 5    16 ] 7Q
 3Q  [ 6    15 ] 6Q
 3D  [ 7    14 ] 6D
 4D  [ 8    13 ] 5D
 4Q  [ 9    12 ] 5Q
GND  [10    11 ] LE
```

SN54AC373 . . . FK PACKAGE
(TOP VIEW)

```
          1D  1Q  OE  V_CC  8Q
           3   2   1  20   19
  2D [ 4                      18 ] 8D
  2Q [ 5                      17 ] 7D
  3Q [ 6                      16 ] 7Q
  3D [ 7                      15 ] 6Q
  4D [ 8                      14 ] 6D
            9  10  11  12  13
          4Q  GND  LE  5Q  5D
```
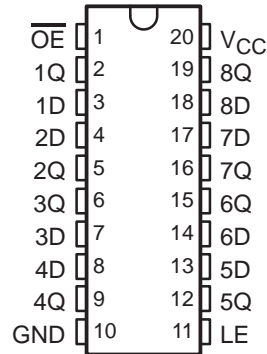
description/ordering information

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are D-type transparent latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.
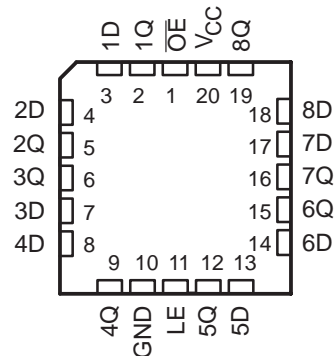
A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines in bus-organized systems without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP – N	Tube	SN74AC373N	SN74AC373N
	SOIC – DW	Tube	SN74AC373DW	AC373
		Tape and reel	SN74AC373DWR	
	SOP – NS	Tape and reel	SN74AC373NSR	AC373
	SSOP – DB	Tape and reel	SN74AC373DBR	AC373
	TSSOP – PW	Tube	SN74AC373PW	AC373
		Tape and reel	SN74AC373PWR	
−55°C to 125°C	CDIP – J	Tube	SNJ54AC373J	SNJ54AC373J
	CFP – W	Tube	SNJ54AC373W	SNJ54AC373W
	LCCC – FK	Tube	SNJ54AC373FK	SNJ54AC373FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

SN54AC373, SN74AC373
OCTAL D-TYPE TRANSPARENT LATCHES
WITH 3-STATE OUTPUTS

SCAS540D – OCTOBER 1995 – REVISED OCTOBER 2003

description/ordering information (continued)

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)

To Seven Other Channels
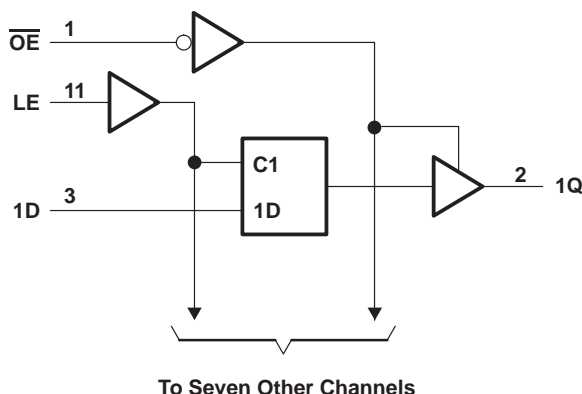
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} .... −0.5 V to 7 V

Input voltage range, V_I (see Note 1) .... −0.5 V to V_{CC} + 0.5 V

Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V

Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) .... ±20 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±20 mA

Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA

Continuous current through V_{CC} or GND .... ±200 mA

Package thermal impedance, θ_{JA} (see Note 2): DB package .... 70°C/W

DW package .... 58°C/W

N package .... 69°C/W

NS package .... 60°C/W

PW package .... 83°C/W

Storage temperature range, T_{stg} .... −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54AC373 MIN	SN54AC373 MAX	SN74AC373 MIN	SN74AC373 MAX	UNIT
V_{CC}	Supply voltage		2	6	2	6	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1		2.1		V
		V_{CC} = 4.5 V	3.15		3.15		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 3 V		0.9		0.9	V
		V_{CC} = 4.5V		1.35		1.35	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V		−12		−12	mA
		V_{CC} = 4.5 V		−24		−24	
		V_{CC} = 5.5 V		−24		−24	
I_{OL}	Low-level output current	V_{CC} = 3 V		12		12	mA
		V_{CC} = 4.5 V		24		24	
		V_{CC} = 5.5 V		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			8		8	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3:   All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$ MIN	TYP	MAX	SN54AC373 MIN	MAX	SN74AC373 MIN	MAX	UNIT
V_{OH}	I_{OH} = −50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −12 mA	3 V	2.56			2.4		2.46		
	I_{OH} = −24 mA	4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
V_{OL}	I_{OL} = 50 µA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	µA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±5		±2.5	µA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		80		40	µA
C_i	$V_I = V_{CC}$ or GND	5 V		4.5						pF

SN54AC373, SN74AC373
OCTAL D-TYPE TRANSPARENT LATCHES
WITH 3-STATE OUTPUTS

SCAS540D – OCTOBER 1995 – REVISED OCTOBER 2003

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AC373		SN74AC373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	5.5		6.5		6		ns
t_{su}	Setup time, data before LE↓	5.5		6.5		6		ns
t_h	Hold time, data after LE↓	1		1		1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AC373		SN74AC373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	4		5		4.5		ns
t_{su}	Setup time, data before LE↓	4		5		4.5		ns
t_h	Hold time, data after LE↓	1		1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	TO (INPUT)	TO (OUTPUT)	T_A = 25°C			SN54AC373		SN74AC373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1.5	10	13.5	1	16.5	1.5	15	ns
t_{PHL}			1.5	9.5	13.0	1	16	1.5	14.5	
t_{PLH}	LE	Q	1.5	10	13.5	1	16.5	1.5	15	ns
t_{PHL}			1.5	9.5	12.5	1	15	1.5	14	
t_{PZH}	$\overline{OE}$	Q	1.5	9	11.5	1	14	1	13	ns
t_{PZL}			1.5	8.5	11.5	1	13.5	1	13	
t_{PHZ}	$\overline{OE}$	Q	1.5	10	12.5	1	16	1	14.5	ns
t_{PLZ}			1.5	8	11.5	1	13	1	12.5	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER	TO (INPUT)	TO (OUTPUT)	T_A = 25°C			SN54AC373		SN74AC373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1.5	7	9.5	1	11.5	1.5	10.5	ns
t_{PHL}			1.5	7	9.5	1	11.5	1.5	10.5	
t_{PLH}	LE	Q	1.5	7.5	9.5	1	12	1.5	10.5	ns
t_{PHL}			1.5	7	9.5	1	11	1.5	10.5	
t_{PZH}	$\overline{OE}$	Q	1.5	7	8.5	1	10.5	1	9.5	ns
t_{PZL}			1.5	6.5	8.5	1	10	1	9.5	
t_{PHZ}	$\overline{OE}$	Q	1.5	8	11	1	13.5	1	12.5	ns
t_{PLZ}			1.5	6.5	8.5	1	10.5	1	10	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	40	pF

![Texas Instruments logo]

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION
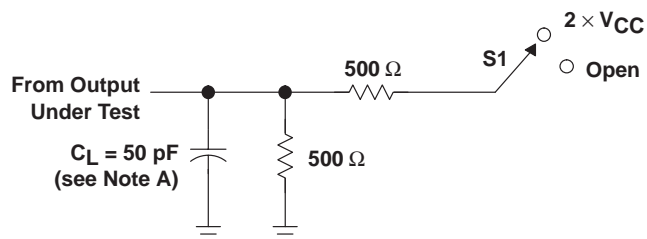
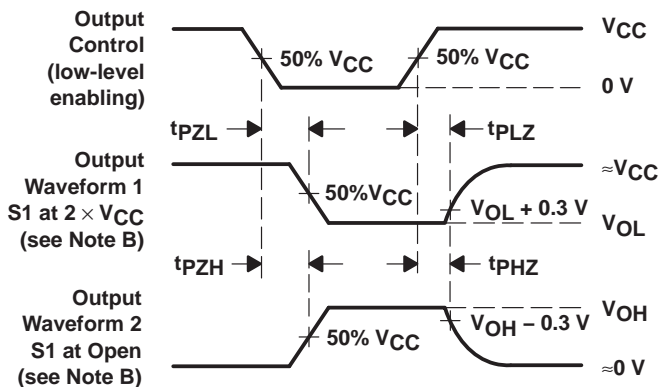| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT
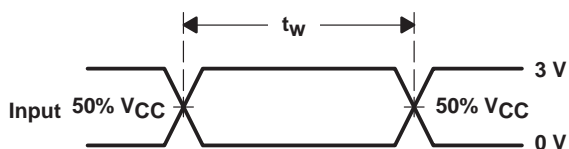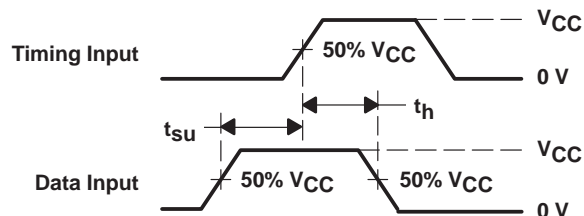
VOLTAGE WAVEFORMS
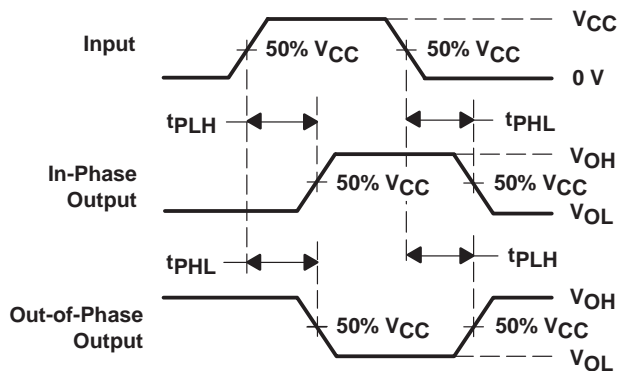
VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
   D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

TEXAS
INSTRUMENTS

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-87555012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8755501RA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8755501SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
5962-8755501VRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8755501VSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
SN74AC373DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
SN74AC373DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AC373NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AC373NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI
SN74AC373PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54AC373FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SNJ54AC373J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54AC373W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54AC373, SN54AC373-SP, SN74AC373 :
● Enhanced Product: SN74AC373-EP

NOTE: Qualified Version Definitions:

● Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC373DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AC373DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74AC373NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74AC373PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC373DBR	SSOP	DB	20	2000	346.0	346.0	33.0
SN74AC373DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74AC373NSR	SO	NS	20	2000	346.0	346.0	41.0
SN74AC373PWR	TSSOP	PW	20	2000	346.0	346.0	33.0

DB (R-PDSO-G**) **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
   B.   This drawing is subject to change without notice.
   C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R—GDIP—T**)   CERAMIC DUAL IN—LINE PACKAGE
14 LEADS SHOWN

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

$\frac{0.065\ (1,65)}{0.045\ (1,14)}$

0.005 (0,13) MIN

$\frac{0.060\ (1,52)}{0.015\ (0,38)}$

A

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

$\frac{0.026\ (0,66)}{0.014\ (0,36)}$

0.100 (2,54)

0°—15°

$\frac{0.014\ (0,36)}{0.008\ (0,20)}$

4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package is hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E.   Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

PW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
          D. Falls within JEDEC MO-153

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

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POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

W (R–GDFP–F20)   CERAMIC DUAL FLATPACK

Base and Seating Plane

$\frac{0.045\ (1,14)}{0.026\ (0,66)}$

$\frac{0.300\ (7,62)}{0.245\ (6,22)}$

$\frac{0.009\ (0,23)}{0.004\ (0,10)}$

$\frac{0.100\ (2,45)}{0.045\ (1,14)}$

0.320 (8,13) MAX

1   20

0.540 (13,72) MAX

$\frac{0.022\ (0,56)}{0.015\ (0,38)}$

0.050 (1,27)

0.005 (0,13) MIN
4 Places

10   11

$\frac{0.370\ (9,40)}{0.250\ (6,35)}$ $\frac{0.370\ (9,40)}{0.250\ (6,35)}$

4040180–4/D 07/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package can be hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only.
         E. Falls within Mil–Std 1835 GDFP2–F20

DW (R−PDSO−G20)　　　　　　　　PLASTIC SMALL−OUTLINE PACKAGE

0.512 (13,00)
0.496 (12,60)

20　　　　　　　　　　　　　　11

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1　　　　　　　　　　　　　10

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

⌒ | 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−4/F 06/2004

NOTES:　A.　All linear dimensions are in inches (millimeters).
　　　　　B.　This drawing is subject to change without notice.
　　　　　C.　Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
　　　　　D.　Falls within JEDEC MS−013 variation AC.

N (R−PDIP−T**)
16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) ⚠D

0.045 (1,14) / 0.030 (0,76) ⚠D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option ⚠D

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
⚠C Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
⚠D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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